REMARKS

Applicant is in receipt of the Office Action mailed January 4, 2005. FIG. 7 has been changed to correct a typographical error. Claim 17, and claims 20-24 have been cancelled. New claims 25 and 26 have been added. Claims 1-16, 18-19, and 25-26 are pending. Reconsideration of the present case is earnestly requested in light of the following remarks.

Claim Objections:

Claims 2, 5, 7-8, 10, 13, 15, 18, 20, 22, and 24 were objected to because of informalities. Claims 20, 22, and 24 have been cancelled, thus objection to those claims is rendered moot. The remaining objected to claims have been amended to correct the informalities.

35 U.S.C. § 112 Rejection:

Claims 1-15 were objected to under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. The specific antecedent problems and incorrect punctuation pointed out by the Examiner, and pertaining to claims 1-15, have been corrected to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

35 U.S.C. § 102 Rejection:

Claims 1, 5, 8-9, 13, and 15-24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wu, U.S. Patent 6,002,276. Claims 17, and 20-24 have been cancelled, thus rejection of those claims is rendered moot. New claims 25 and 26 have been added.

With respect to the remaining claims and the new claims, Applicant respectfully traverses this rejection.

Applicant has amended claims 1-16 and claims 18-19, and added new claims 25-26 to more clearly and distinctly claim the invention. **The cited reference does not teach or suggest all of the elements of independent claim 1.**

As currently amended, independent claim 1 of Applicant recites:

1. A device comprising:

a voltage level detector comprising an NMOS tail current transistor; and

a voltage generator coupled to a gate of the tail current transistor;

wherein the voltage generator is configured to deliver a voltage to the gate of the tail current transistor;

wherein a first component of the voltage is approximately equal to a threshold voltage (Vt) of NMOS transistors comprised in the device; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters.

The cited reference does not teach or suggest a voltage generator "configured to deliver a voltage to the gate of the tail current transistor; wherein a first component of the voltage is approximately equal to a threshold voltage (Vt) of NMOS transistors comprised in the device; and wherein a second component of the voltage is approximately constant with respect to variations in operating temperature as well as variations in transistor fabrication parameters", as further outlined in detail below.

The Examiner, referencing FIG. 1 of Wu, states that Wu shows a device comprising a voltage detector comprising a tail current transistor M9; and voltage generator M1-M6 coupled to deliver a voltage (on line 12) to the gate of tail current transistor M9. When referring to FIG. 1 of Wu, Examiner states that the voltage at line 12 comprises a first component equivalent to the threshold voltage of diode-connected

NMOS transistor M3, and a second component equivalent to the threshold voltage of diode-connected NMOS transistor M4, which is considered approximately constant with respect to variations in operating temperature as well as transistor fabrication parameters. This characterization, however, is incorrect.

It is clear from the specifications set forth in Wu, that M1-M6 form a bias circuit commonly used to provide bias voltage on conductors 12 and 13 to drive current mirror output transistors such as M9 and M10 in FIG. 1, where the current mirror output transistors function as a constant current source for a differential amplifier stage 3. (Column 1, lines 61-66.) In contrast, the current flowing in NMOS tail current transistor as claimed by applicant in claim 1, for example, is not constant. By providing a first component of the voltage that "is approximately equal to a threshold voltage (Vt) of NMOS transistors comprised in the device" and a second component of the voltage that "is approximately constant with respect to variations in operating temperature as well as variations in transistor fabrication parameters", the current flowing in the tail current transistor will actually be proportional to the beta of the NMOS process, as described, for example, in paragraph 0009 on page 4 of Applicant's originally submitted specifications.

In contrast, the current flowing in a first leg of the bias circuit of FIG.1 of Wu, which includes resistor R1 and MOSFETs M2, M3, and M4, is approximately equal to the P-channel threshold voltage V_{TP} of MOSFET M1 divided by the resistance R1 of resistor R1 (Column 5, lines 20-23). Consequently, the current through resistor R1, multiplied by the scale factor k, then flows through the constant current source MOSFETs M9 and M10 of error amplifier 3 (Column 5, lines 32-34). Since the current through NMOS M9 is determined by the P-channel threshold voltage V_{TP} of MOSFET M1 divided by the resistance R1 of resistor R1, the voltage at node 12 is not comprised of the threshold voltage of NMOS transistor M3 and the threshold voltage of NMOS transistor M4 as erroneously stated by Examiner. Furthermore, no compensation is present in the circuit disclosed by Wu that would insure that the threshold voltage of NMOS transistor M4 remains constant with respect to variations in operating temperature as well as transistor fabrication parameters.

Therefore, Wu does not teach or suggest applying a combined voltage to the gate of the tail-current transistor, where the "second component of the voltage is

approximately constant with respect to variations in operating temperature as well as variations in transistor fabrication parameters". Furthermore, because the main aim of Wu is to provide a low-impedance CMOS output stage which can be used to provide large output voltage swings into low impedance loads and steady DC bias current in the output transistors of such output stage over typical variations in power supply voltage, CMOS processing parameters, and chip temperature (Column 2, lines 20-26), there is no motivation to provide the subject matter of claim 1.

For at least these reasons, Applicant submits that the combinations of features recited in independent claim 1 are not anticipated or rendered obvious by Wu. With regard to claims 9 and 16, Applicant submits that claims 9 and 16 are allowable based on the arguments presented above for claim 1. Accordingly, Applicant respectfully requests removal of the 35 U.S.C. § 102(b) rejection. Applicant submits that claims 2-8 are allowable based on their dependence on allowable claim 1, claims 10-15 are allowable based on their dependence on allowable claim 9, and claims 18-19, and 25-26 are allowable based on their dependence on allowable claim 16.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5707-04100/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

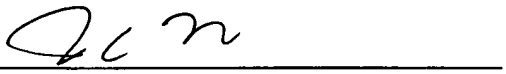
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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IN THE DRAWINGS:

The attached replacement sheet contains a formal drawing that includes changes to FIG. 7. This sheet replaces the originally filed sheet containing the same figure.

Attachment: 1 replacement sheet and 1 sheet illustrating the change to FIG. 7 of the original drawing.

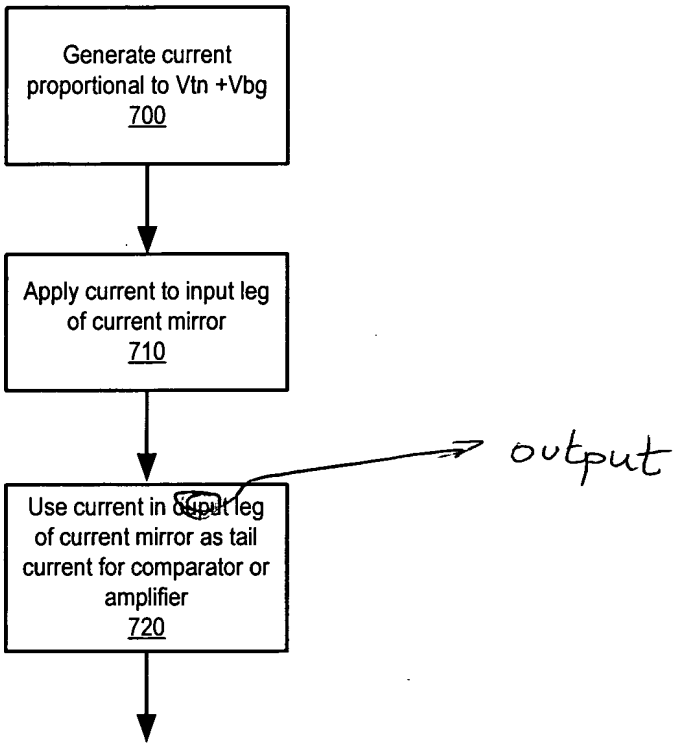

FIG. 7